

A Manufacturing Process for Analog and Digital Gallium Arsenide Integrated Circuits

R.L. Van Tuyl, V. Kumar, D.C. D'Avanzo, T.W. Taylor, V.E. Peterson, D.P. Hornbuckle, R.A. Fisher and D.B. Estreich. "A Manufacturing Process for Analog and Digital Gallium Arsenide Integrated Circuits." 1982 *Transactions on Microwave Theory and Techniques* 30.7 (Jul. 1982 [T-MTT] (Joint Special Issue on GaAs IC's)): 935-942.

A process for manufacturing small-to-medium scale GaAs integrated circuits is described. Integrated FET's, diodes, resistors, thin-film capacitors, and inductors are used for monolithic integration of digital and analog circuits. Direct implantation of Si into $>10^{15}$ Ω/cm^2 resistivity substrates produces n-layers with ± 10 -percent sheet resistance variation. A planar fabrication process featuring retained anneal cap (SiO_2), proton isolation, recessed Mo-Au gates, silicon nitride passivation, and a dual-level metal system with polyimide intermetal dielectric is described. Automated on-wafer testing at frequencies up to 4 GHz is introduced, and a calculator-controlled frequency domain test system described. Circuit yields for six different circuit designs are reported, and process defect densities are inferred.

 [Return to main document.](#)